What is claimed is:

Sub A10 Cont'd

1. A matching circuit for absorbing fluctuation of electric characteristics of a transistor, comprising:

a capacitor having a capacity that increases and decreases contrarily to increment and decrement of a parasitic capacity around said transistor.

2. The matching circuit according to claim 1,

wherein said parasitic capacity increases and decreases according to a thickness change of an MIM insulation film formed around said transistor and said capacitor has an MIM capacity to increase and decrease contrarily to the increment and decrement of said parasitic capacity.

3. The matching circuit according to claim 2,

wherein said capacitor is provided at an input side of said transistor.

4. The matching circuit according to claim 3,

wherein said matching circuit is provided with a predetermined bias circuit disposed in parallel to said capacitor provided at the input side of said transistor.

5. The matching circuit according to claim 2,

wherein said capacitor is provided at an output side of said transistor.

6. The matching circuit according to claim 5,

wherein said matching circuit is provided with a predetermined bias circuit disposed in parallel to said capacitor provided at the output side of said transistor.

7. The matching circuit according to claim 1,

wherein said capacitor is provided at an input side of said transistor.

8. The matching circuit according to claim 7,

wherein said matching circuit is provided with a predetermined bias circuit disposed in parallel to said capacitor provided at the input side of said transistor.

9. The matching circuit according to claim 1,

wherein said capacitor is provided at an output side of said transistor.

10. The matching circuit according to claim 9,

wherein said matching circuit is provided with a predetermined bias circuit disposed in parallel to said capacitor provided at the output side of said transistor.

11. A semiconductor device fabricated with use of said matching circuit according to claim 1.

12. A semiconductor device fabricated with use of said matching circuit according to claim 2.